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14.3 A Push-Pull mm-Wave Power Amplifier with <0.8° AM-PM Distortion in 40nm CMOS

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Millimeter-Wave standards like IEEE 802.15.3c and the new 802.11ad have classifications of their PHY to support single-carrier mode and more complex OFDM mode (high-speed interface) with high peak-to-average ratio (PAPR). To improve the efficiency of power amplifiers (PA), the trend is towards Class-AB and Class-B PAs that exhibit better energy efficiency compared to Class-A. However, Class-AB and -B biasing brings along large amplitude-to-phase-modulation (AM-PM) distortion which degrades EVM and ACPR. At the same time, PMOS transistors become attractive in nanometer CMOS as their f_{MAX} exceeds 140GHz. This makes it possible to use both NMOS and PMOS transistors at mm-Wave frequencies. This paper presents a 60GHz complementary Push-Pull PA, using both NMOS and PMOS transistors. An inverter-like architecture which uses both PMOS and NMOS results in the cancellation of AM-PM distortion which is particularly important in high-fidelity amplification of OFDM systems and high-order modulation schemes like 16- and 64-QAM, which are very sensitive to phase distortion. Furthermore, the complementary nature allows deep Class-AB operation, giving a high power efficiency at power back-off comparable to state-of-the-art 60GHz PA structures based on NMOS only.

Figure 14.3.1 shows the complete architecture of the PA. At the output, a transformer-based combiner is employed, which has two differential excitation ports on the primary side and a standard secondary winding connected to the output pads [1]. The combiner has an insertion loss of only 1dB at 62GHz. The PA consists of two stages of Push-Pull unit amplifiers, making use of both NMOS and PMOS, progressively sized with interstage transformers. A common—gate (CG) buffer stage is used at the input as it provides lower input impedance and can be matched to 50Ω easily [2]. The CG buffer only compensates for the loss in the input power divider.

The Push-Pull PA consists of a differential inverter-like structure shown in Fig 14.3.2. To enable deep Class-AB operation and cancellation of the AM-PM, the bias levels of the PMOS and NMOS are set independently. Therefore, an interstage power splitter that consists of a transformer with two secondary windings with separate DC center-tap access is designed as shown in Fig 14.3.2. As the PMOS is sized 30% larger than the NMOS, its input susceptance is larger than the NMOS. Hence it is tuned by the inner secondary winding. The input impedance of the PMOS and NMOS are different and they are matched to the previous stage by optimizing the width and overlap of the two secondary windings with the primary winding. In each Push-Pull unit PA, individual neutralization capacitors are adopted for the PMOS and NMOS (C_P,C_N) separately so as not to disturb their DC bias. This helps to improve the stability and reverse isolation at mm-Wave frequencies.

The two major benefits of using complementary Push-Pull PAs is their ability to minimize AM-PM distortion and their low quiescent current for a given RF output power. One of the primary causes for AM-PM distortion is the nonlinear input capacitance of the transistor [3]. As the input RF amplitude increases the average value of C_{GS} will change, thus causing AM-PM distortion. To counter this type of distortion, additional circuitry is often added to balance the phase change [3,4]. However, the changes of input capacitance for PMOS and NMOS are in opposite directions because of their complementary nature as shown in Fig. 14.3.3. As such, both the NMOS and PMOS show a fairly large amount of AM-PM distortion which is often a problem in mm-Wave NMOS-only deep Class-AB PAs [5]. But when the NMOS and PMOS drain currents are summed up, the distortion is cancelled and the effective AM-PM can be minimized up to and beyond the 1dB compression point (P_{1dB}). This is a major benefit of the proposed PA, which enables amplification of large PAPR signals like 64-QAM with low EVM. Figure 14.3.3 also shows the measured AM-AM and AM-PM at 63GHz which is below 0.25° up to P_{1dB}. This demonstrates the excellent phase linearity of the PA, which is required to support a large number of constellation points.

The last-stage transistors are biased very close to their threshold voltage for deep Class-AB operation. As a result the quiescent current consumption is small for low output power and goes up only when more RF output power is to be delivered. This change in current is more than three times for low-to-high RF output power levels as shown in Fig. 14.3.4. This second benefit is a direct manifestation of the complementary behavior of the Push-Pull PA. Because of this, the measured peak drain efficiency (DE) is larger than 40% as shown in Fig. 14.3.4.

The prototype PA is fabricated in a 0.9V 40nm GP 1P10M digital CMOS process. The 60GHz power measurement results are shown in Fig. 14.3.4. The quiescent voltage at the drains of the Push-Pull stage are at half of their supply voltage. Due to stacking of two transistors in the Push-Pull stage, their supply is maintained at 1.8V. In this configuration, the transistors face similar stress as conventional NMOS-only-based PAs, whereas the CG buffer stage uses 0.9V supply for reliable operation. Under these conditions, the measured gain is 22.4dB, P_{1dB} is 13.9dBm and the saturated output power (P_{SAT}) is 16.4dBm at 63GHz. The measured peak DE is 40.9%, peak PAE is 23% and PAE at P_{1dB} is 18.9%. The DC power profile clearly shows that the PA operates in deep Class-AB mode. Figure 14.3.4 also shows the individual current consumption of all the stages. The DC power consumption more than halves in the low-power region compared to saturated power. The PA maintains P_{SAT} above 15dBm, P_{1dB} above 10dBm and peak PAE above 16% in the band from 59 to 67GHz.

Figure 14.3.5 shows the measured AM-PM distortion at P_{1dB}, which is below 0.8° across the band of 59 to 67GHz. It also shows the measurement result when a high-order constellation modulated signal is applied to the PA. With a 64-QAM signal at 63GHz, an EVM of -25.2dB is measured for a data-rate of 3Gb/s with 7dBm average output power. This signal uses a raised-cosine shaped filter with a rolloff factor of 0.35 and has 8.1dB of PAPR. Achieving such wideband linearity is due to the complementary Push-Pull technique that minimizes AM-PM distortion.

Figure 14.3.6 summarizes the comparison with state-of-the-art mm-Wave PAs employed in transmitters. The proposed PA, which employs a complementary Push-Pull technique, uses AM-PM cancellation and is capable of amplifying 64-QAM signal and at the same time maintaining state-of-the-art PAE at 5dB backoff from P_{1dB}. Figure 14.3.7 shows the die photo of the PA with a total area of 0.4mm² including the pads, while the active area is only 0.0812mm².

Acknowledgments:
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References:
[1] J. Chen, A. Niknejad, "A Compact 1V 18.6dBm 60GHz Power Amplifier in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 432-433, Feb. 2011.
[2] D. Zhao, S. Kulkarni, P. Reynaert, "A 60-GHz Outphasing Transmitter in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol.47, pp. 3172-3183, Dec. 2012.
[3] Y. Palaskas et al., "A 5GHz 20dBm Power Amplifier with Digitally Assisted AM-PM Correction in a 90nm CMOS Process," *IEEE J. Solid-State Circuits*, vol.37, pp.1757-1763, Aug. 2006.
[4] J. Chen et al., "A Digitally Modulated mm-Wave Cartesian Beamforming Transmitter with Quadrature Spatial Combining," *ISSCC Dig. Tech. Papers*, pp. 232-233, Feb. 2013.
[5] D. Zhao, P. Reynaert, "A 60-GHz Dual-Mode Class AB Power Amplifier in 40-nm CMOS," *IEEE J. Solid State Circuits*, vol.48, pp. 2323-2337, Oct. 2013.
[6] V. Vidojkovic et al., "A Low-Power Radio Chipset in 40nm LP CMOS with Beamforming for 60GHz High-Data-Rate Wireless Communication," *ISSCC Dig. Tech. Papers*, pp. 236-237, Feb. 2013.
[7] K. Okada et al., "A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE802.15.3c," *IEEE J. Solid-State Circuits*, vol.46, pp. 2988-3004, Dec. 2011.
[8] A. Siligaris et al., "A 65nm CMOS Fully Integrated Transceiver Module for 60GHz Wireless HD Applications," *ISSCC Dig. Tech. Papers*, pp.162-164, Feb. 2011.

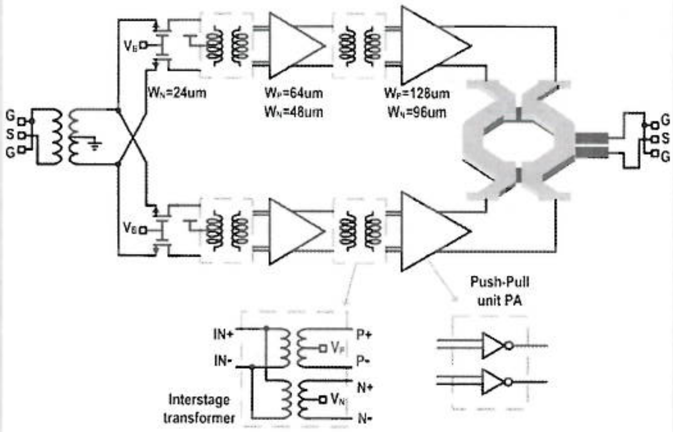

Figure 14.3.1: Architecture of the complementary Push-Pull power amplifier along with the output power combiner.

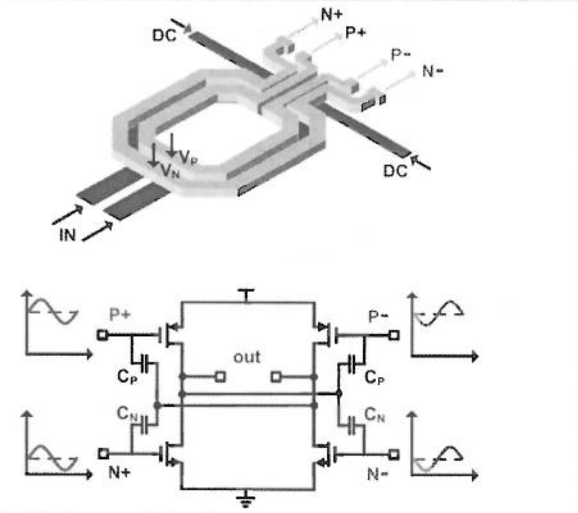

Figure 14.3.2: Layout of the interstage transformer; schematic of the complementary Push-Pull unit PA.

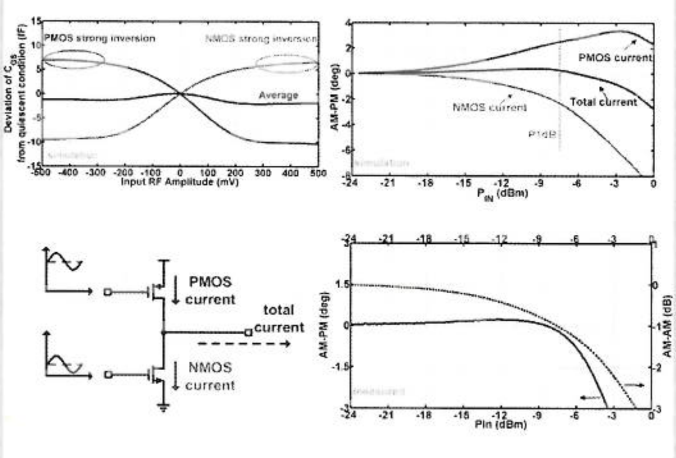

Figure 14.3.3: Variation of C_{GS} due to input RF amplitude; and its impact on AM-PM; measured AM-AM and AM-PM at 63GHz.

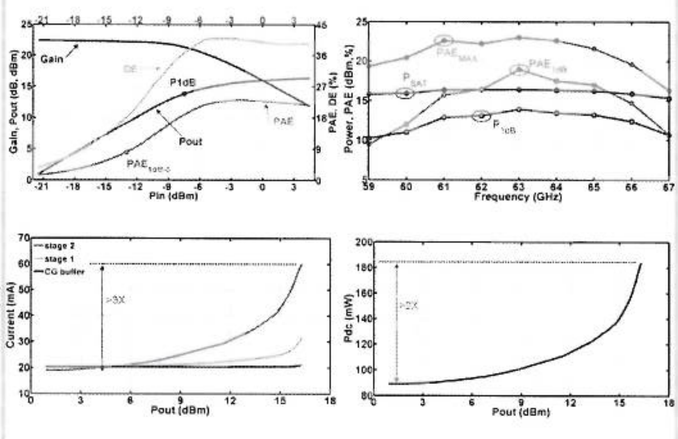

Figure 14.3.4: Measured gain, output power, DE and PAE over the band 59 to 67GHz; DC current and power consumption measured at 63GHz.

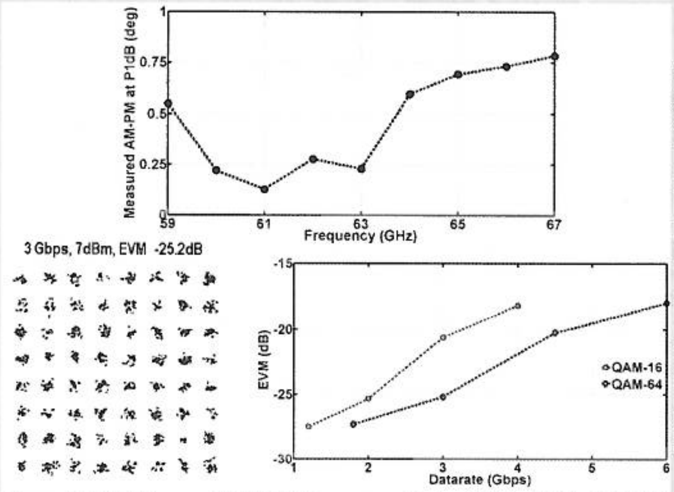

Figure 14.3.5: Measured AM-PM at P_{1dB} across the band 59 to 67GHz, 64-QAM constellation at a data-rate of 3Gb/s at 63GHz and 7dBm P_{AVG}; modulated signal performance.

	This work	[2]	[6]	[7]	[8] (w/o offchip pa)	[1]	[5]
Tech (nm)	40	40	40	65	65	65	40
Gain (dB)	22.4	26	22.5	18.3	16.4	20.3	17
P_{SAT} (dBm)	16.4	15.6	10	10.9	13	18.6	17
P_{1dB} (dBm)	13.9	15.6	8	9.5	8	15	13.8
PAE_{max} (%)	23	25	22.5	8.8	8	15.1	30.3
PAE_{1dB} (%)	18.9	25	16	< 8.8	< 8	6.8	21.6
$PAE_{1dB\text{-}6}$ (%)	8	10	7.4	2.5	NA	2	8.4
AM-PM (deg)	0.2°	15°	-	-	-	-	0.2° AB / > 3° deep AB
modulated signal	QAM-64	QAM-16	QAM-16	QAM-16	OFDM QAM16	-	-

Figure 14.3.6: Comparison with state-of-the-art 60GHz PAs with modulated signal measurements.